

Amendments to the Claims

This listing of claims will replace all prior versions, and listings, of claims in the application.

1. (Currently Amended) A method of communicating across a distributed multiprocessing system having a first node with a first processor and a first real memory location and a second node with a second processor and a second real memory location, the first and second nodes are connected to a central signal routing hub by first and second communication links, respectively, said method comprising the steps of;

indexing the first and second nodes to define different destination addresses for each of the nodes;

processing information within the first processor of the first node for creating data;

addressing the data processed information using at least one of the destination addresses;

transmitting the data processed information from the first processor of the first node across the first communication link toward the hub without storing the data processed information in the first real memory location of the first node, thereby defining a sending node;

receiving the data processed information along with the destination address within the hub;

identifying the destination address for the transmitted data processed information within the hub;

sending the data processed information without modification from the hub over at least one of the communication links to at least one of the first and second nodes associated with the destination address, thereby defining at least one addressed node; and

storing the data processed information within the real memory location of the addressed node.

2. (Cancelled).

3. (Currently Amended) A method as set forth in claim [[2]] 1 wherein the step of processing information is further defined as compiling the data within the first processor.

4. (Currently Amended) A method as set forth in claim [[2]] 1 wherein the step of transmitting the data processed information is further defined as transmitting the data along with executable code from the sending node to the addressed node.

5. (Currently Amended) A method as set forth in claim 3 wherein the step of transmitting the data processed information is further defined as transmitting the data processed information across the first communication link in only one direction from the first processor to the hub to define a send-only system.

6. (Currently Amended) A method as set forth in claim 5 wherein the step of sending the data processed information without modification is further defined as sending the data processed information from the hub over at least one of the communication links in only one direction from the hub to at least one of the first and second nodes to further define the send-only system.

7. (Currently Amended) A method as set forth in claim 1 further including the step of directing the first processor to a subsequent task to be performed while simultaneously sending the data processed information across the first communication link to the hub.

8. (Previously Presented) A method as set forth in claim 1 wherein the step of indexing the first and second nodes is further defined as indexing the nodes to define an identifier for each of the nodes for differentiating the nodes.

9. (Currently Amended) A method as set forth in claim 8 further including the step of creating a virtual memory map of each of the identifiers within each of the first and

second nodes such that the first and second nodes can address and forward data processed information to each of the indexed nodes within the system.

10. (Currently Amended) A method as set forth in claim 9 wherein the step of addressing the data processed information is further defined as assigning a destination address onto the data processed information corresponding to the identifier of the addressed node.

11. (Cancelled).

12. (Currently Amended) A method as set forth in claim 1 wherein the step of addressing the data processed information further comprises the step of assigning a memory address onto the data processed information corresponding to a location of the real memory location of the addressed node.

13. (Cancelled).

14. (Previously Presented) A method as set forth in claim 8 further including the step of interconnecting the hub to a second hub, having third and fourth nodes, by a hub link.

15. (Original) A method as set forth in claim 14 further including the step of indexing the hubs to define a master hub and a secondary hub.

16. (Previously Presented) A method as set forth in claim 15 further including the step of indexing the first, second, third, and fourth nodes in accordance with the master and secondary hub indexes to redefine the identifiers for each of the nodes such that each of the nodes can be differentiated.

17. (Currently Amended) A method as set forth in claim 16 further including the step of simultaneously sending the data processed information to all of the indexed nodes by simultaneously placing the destination addresses of each of the indexed nodes onto the sent information.

18. (Currently Amended) A method as set forth in claim 17 further including the step of limiting the number of times that the data processed information can be sent from a sending nodes.

19. (Currently Amended) A distributed multiprocessing system comprising;
a first node and a second node with said nodes being separated from each other,
a first processor disposed within said first node for processing information, creating data and for assigning a first address to a first set of data processed information,
a first real memory location disposed within said first node for storing data processed information at said first node,
a second processor disposed within said second node for processing information, creating data and for assigning a second address to a second set of data processed information,
a second real memory location disposed within said second node for storing data processed information at said second node,
a central signal routing hub,
an indexer connected to said routing hub for indexing said first and second nodes to define different destination addresses for each of said nodes,
a first communication link interconnecting said first node and said hub for transmitting said first set of data processed information between said first processor of said first node and said hub without storing said first set of data processed information within said first real memory location of said first node,
a second communication link interconnecting said second node and said hub for transmitting said second set of data processed information between said second processor of said second node and said hub without storing said second set of data processed information.

information within said second real memory location of said second node,

 said central routing hub including a sorter for receiving at least one of said first and second sets of data processed information from at least one of said first and second nodes, thereby defining at least one sending node, and for associating a destination of at least one of said first and second addresses of said first and second sets of data processed information, respectively, with at least one of said destination addresses, and for sending at least one of said first and second sets of data processed information without modification from said hub over at least one of said communication links to at least one of said first and second nodes node associated with said destination address, thereby defining at least one addressed node, with said first and second real memory locations only storing said sent set of data processed information received from said hub.

20. (Original) A system as set forth in claim 19 wherein said first communication link includes first incoming and first outgoing transmission lines.

21. (Original) A system as set forth in claim 20 wherein said second communication link includes second incoming and second outgoing transmission lines.

22. (Original) A system as set forth in claim 21 wherein said first and second incoming transmission lines interconnect said first and second processors, respectively, to said hub for transmitting signals in only one direction from said first and second processors to said hub to define a send-only system.

23. (Original) A system as set forth in claim 22 wherein said first and second outgoing transmission lines interconnect said first and second processors, respectively, to said hub for transmitting signals in only one direction from said hub to said first and second processors to further define said send-only system.

24. (Original) A system as set forth in claim 23 wherein said first and second incoming transmission lines and said first and second outgoing transmission lines are

unidirectional optical fiber links.

25. (Previously Presented) A system as set forth in claim 19 further including at least one actuator connected to at least one of said first and second nodes, respectively, for performing a testing operation during an operation of said system.

26. (Original) A system as set forth in claim 25 wherein said actuator is further defined as servo-hydraulic actuator.

27. (Previously Presented) A system as set forth in claim 19 wherein said indexer defines an identifier for each of said nodes for differentiating said nodes.

28. (Currently Amended) A system as set forth in claim 27 wherein said first and second nodes each include virtual memory maps of each identifier such that said first and second processors can address and forward data processed information to each of said indexed nodes within said system.

29. (Original) A system as set forth in claim 28 wherein each of said first and second processors further include a hardware portion for assigning said first and second addresses to said first and second processed information, respectively.

30. (Currently Amended) A system as set forth in claim 29 wherein said hardware portion assigns a destination address onto said data processed information corresponding to said identifier of said addressed node.

31. (Previously Presented) A system as set forth in claim 30 wherein said first real memory location is connected to said hardware portion of said first processor and said second real memory location is connected to said hardware portion of said second processor.

32. (Currently Amended) A system as set forth in claim 31 wherein said hardware portion assigns a memory address onto said data processed information corresponding to a location of an associated first and second real memory location of said addressed node.

33. (Previously Presented) A system as set forth in claim 27 further including a second hub, having third and fourth nodes, interconnected to said first hub by a hub link.

34. (Previously Presented) A system as set forth in claim 33 wherein said indexer indexes said first and second hubs to define a master hub and secondary hub and indexes said first, second, third, and fourth nodes to redefine said identifiers for each of said nodes for differentiating said nodes.

35. (Original) A system as set forth in claim 34 further including a key disposed within one of said first and second hubs to determine which of said hubs will be defined as said master hub.

36. (Original) A system as set forth in claim 19 wherein each of said first and second processors further include at least one task.

37. (Currently Amended) A system as set forth in claim 36 wherein said processors include executable code for processing information defined by each of said tasks and creating said data.

38. (Currently Amended) A system as set forth in claim 37 wherein said task includes at least a pair of pointers for directing a flow of said data from said sending node to said destination node.

39. (Currently Amended) A system as set forth in claim 38 wherein said pointers includes a next task pointer for directing said sending processor to a subsequent task to be performed, and at least one data destination pointer for directing said first and second

processor associated with said sending node to send said data processed information across said first communication link to said hub.

40. (Currently Amended) A system as set forth in claim 39 wherein said at least one data destination pointer includes a plurality of data destination pointers to direct said first and second processor associated with said sending node to simultaneously forward data processed information to a plurality of addressed nodes.

41. (Original) A system as set forth in claim 39 further including a chipset interconnected between each of said incoming and outgoing communication links and said corresponding processors for creating a virtually transparent connection therebetween.

42. (Original) A system as set forth in claim 41 further including a buffer disposed between each of said processors and said chipsets.

43. (Currently Amended) A system as set forth in claim 42 further including a counter for determining a number of times that data processed information is sent to said addressed node.

44. (Original) A system as set forth in claim 43 further including a sequencer for monitoring and controlling a testing operation as performed by said system.

45. (Previously Presented) A system as set forth in claim 19 further including a host computer connected to one of said first and second nodes, said host computer having a processing card and at least one peripheral device.

46. (Original) A system as set forth in claim 45 wherein said peripheral devices are further defined as a monitor, a printer, a key board, and a mouse.

47. (Previously Presented) A system as set forth in claim 19 wherein said sorter includes hardware for determining said destination addresses of said addressed node.

48. - 67. (Cancelled).